IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | | | |
|---|---|---|---|
| Applicant(s): | Om P. Agrawal; Bai Nguyen; Kuang Chi; Brad Sharpe-Geisler; Giap Tran | | |
| Assignee: | Lattice Semiconductor Corporation | | |
| Title: | Scalable Serializer-Deserializer Architecture And Programmable Interface | | |
| Serial No.: | 10/619,645 | Filing Date: | 07/14/2003 |
| Examiner: | Jason Crawford | Group Art Unit: | 2819 |
| Docket No.: | M-15135 US | Confirmation No.: | 9559 |

Irvine, California
March 20, 2006

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**EXHIBIT A FOR**

**37 C.F.R. 1.131 DECLARATION**

LAW OFFICES OF
MACPHERSON KWOK
CHEN & HEID LLP

2402 Michelson Drive
SUITE 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049

# News Release

## Lattice Semiconductor Introduces World's First Infinitely Reconfigurable Instant-On FPGA

***- ispXPGA™ combines Non-volatile and SRAM technologies with advanced high performance mainstream architecture -***

**HILLSBORO, OR - JULY 15, 2002 -** Lattice Semiconductor Corporation (NASDAQ: LSCC), the inventor of in-system programmable (ISP™) logic products, today introduced the industry's first in-system programmable and dynamically reconfigurable Instant-On FPGA family.

The ispXPGA™ (in-system programmable eXpanded Programmable Gate Array) family combines on-chip $E^2$ memory with SRAM cells in a non-volatile architecture which allows infinite reconfiguration. This unique marriage of technologies is named ispXP™, for eXpanded Programmability. Since the ispXP devices in the ispXPGA family self-configure in microseconds at power-up ("Instant On"), they are available to an electronic system during its power-up sequence. The products are highly secure, as well, since on-chip $E^2$ memory means no external bit stream is exposed during configuration, and security bits can inhibit FPGA pattern readback. The family is supported in Lattice's ispLEVER™ integrated, hierarchical CPLD/FPGA design software.

"Lattice is excited to bring innovative programming technology to the FPGA market with a complete, mainstream product offering," said Steven A. Laub, Lattice's President. "Our unique value for customers with our Non-Volatile/Infinitely-Reconfigurable/Instant-On approach overcomes the deficiencies of conventional SRAM FPGAs."

**ispXPGA Capabilities**
The features most sought by users in an FPGA are all built into the ispXPGA family. These include:

- A versatile PFU (Programmable Function Unit)
  - Hardware-accelerated arithmetic and muxing that enhance performance
  - Distributed single-port, dual-port, FIFO, and shift-register memory for local scratchpad needs
  - Wide-gating expansion for operations with up to 20 inputs
  - Two Flip-Flops per Look-Up Table that improve efficiency/speed of library elements, pipelining, and register-retiming for boosting fMAX
- sysMEM™ embedded 4k-bit memory blocks
  - Single-port, dual-port, and FIFO configurations
  - Parity provided for with x9 and x18 support
- Variable-Length-Interconnect™ optimized for performance and efficiency
- sysIO™ input/outputs giving the user a choice of dozens of I/O types for single-ended and differential needs meeting industry standards for varied applications
- sysCLOCK™ phase-locked-loops (PLLs)
  - Clock frequency synthesis
  - Multiple clock generation
  - Clock alignment at either board or device level
  - Programmable delay for fine-tuning of clock signals in 250ps increments
- sysHSI™ (High-Speed Interface) 850 Mbit I/Os with SERDES and clock recovery for handling ultra-fast data streams

- 1.8/2.5/3.3V operation for users' choice of most convenient power supply

**The ispXPGA Family**
The ispXPGA family covers 125K gates to 1.2M gates or 2K to 15K logic elements. Gates are counted using the industry-standard approach. Block RAM goes from 92K to 414K bits, while Distributed RAM reaches from 30K to 246K bits. The family has products from 160 to 496 I/Os, including 4 to 20 sysHSI clock pairs. This range of resources addresses the vast majority of customer design needs. The ispXPGA family is complemented by Lattice's new ispXPLD™ family, also with ispXP technology, announced today (**please see separate Press Release**).

**ispLEVER Software - "The Simple Machine for Complex Design"™**
Release 2.0 of the Lattice ispLEVER design software includes complete support for the ispXPGA and ispXPLD families as well as ORCA□ Field Programmable System Chips (FPSC), ispMACH™ CPLDs, ispGDX□ crosspoint switches, and ispGAL□ SPLDs. Tools added to the ispLEVER software for the ispXPGA family include a floorplanner, timing-driven place and route, a module compiler, core manager, enhanced constraint editor, and expanded timing analysis, plus HTML report browsing.

The overall user interface of the ispLEVER software carries on from prior releases. This maintains the design environment customers are familiar with, and avoids unnecessary new learning. This means customers can get started quickly with v2.0.

Users' preferred HDL design flows are provided for through Lattice's relationship with major EDA tool suppliers. HDL synthesis support is available for Exemplar Leonardo Spectrum, Mentor Design Architect, Synopsys Design Compile and Synplicity Synplify. Simulation support is available for Cadence Verilog-XL; Mentor ModelSim, QuickSim, and QuickVHDL; Synopsys VSS and Chronologic; Viewlogic ViewSim; and multiple sources of VHDL/Vital. Board-level verification support is available for Mentor/Telalogic Tau, Synopsys PrimeTime, and Viewlogic Blast.

**Intellectual Property (IP) Cores**
Lattice has developed in-house LeverCORE™ IP Cores for our customers. These Cores are aimed at Bus, Communications, Memory, and DSP applications. They are parameterized so users can get the Core functionality they desire. Initial Cores include:

| | |
|---|---|
| PCI | PCI Master/Target 64-bit/66MHz |
| | PCI Target 64-bit/66MHz |
| Utopia | PCI Master/Target 64-bit/66MHz |
| | Utopia Level 3 ATM Receive |
| | Utopia Level 3 ATM Transmit |
| | Utopia Level 3 PHY Receive |
| | Utopia Level 3 PHY Transmit |
| POS-PHY | POS PHY Level 3 Link Layer Interface |
| | POS PHY Level 3 Physical Layer Interface |
| DMA | Multi-Channel DMA Controller |
| DDR SDRAM | DDR SDRAM Controller |
| FIR Filters | Loadable Parallel FIR Filter |
| | Loadable Serial FIR Filter |
| Reed-Solomon | Reed-Solomon Encoder |

More Lattice LeverCORE IP Cores are in development now. All LeverCORE IP cores comply with the Reuse

Methodology Manual HDL code development guidelines to maximize their usefulness to our customers. LeverCORE IP cores include testbenches and extensive documentation.

**Price and Availability**
The initial ispXPGA device to be offered is the 1.2 million gate product, which is called the LFX1200 (Lattice, FPGA Product Line, ispXPGA Family, 1200 K-gates). It is being made available in Commercial (0C to 70C) and Industrial (-40C to +85C) temperature grades as well as 1.8V and 2.5/3.3V power supply versions. Samples will be available later in Q3 with production in Q4. It comes in a 900-ball fine-pitch BGA package or a 680-ball thermally-enhanced fine-pitch BGA package. The LFX1200 is priced at $345 per device in thousands.

ispLEVER design software v2.0 is available for customers to begin designs now. Lattice LeverCORE IP cores will be available in free trial versions from our website later this quarter. These trial versions are encrypted and can be simulated with the rest of a customer design.

**Programmability for all Needs**
Lattice now supplies customers with the broadest range of programmable products of any supplier, making shorter time-to-market achievable in more and more ways. We now offer programmable logic products that include ispXPGA FPGAs, ORCA FPSCs, ispXPLD CPLDs, ispMACH CPLDs, and ispGAL SPLDs; unique ispGDX digital crosspoint switch products; and unique ispPAC programmable analog products. We will continue delivering innovative programmable products to serve customer needs.

**About Lattice Semiconductor**
Oregon-based Lattice Semiconductor Corporation designs, develops and markets the broadest range of high-performance ISP™ programmable logic devices (PLDs), Field Programmable Gate Arrays (FPGAs), and Field Programmable System Chip (FPSC) devices. Lattice offers total solutions for today's system designs by delivering the most innovative programmable silicon products that embody leading-edge system expertise.

Lattice products are sold worldwide through an extensive network of independent sales representatives and distributors, primarily to OEM customers in the fields of communication, computing, computer peripherals, instrumentation, industrial controls and military systems. Company headquarters are located at 5555 NE Moore Court, Hillsboro, Oregon 97124 USA; Telephone 503-268-8000, FAX 503-268-8037. For more information on Lattice Semiconductor Corporation, access our World Wide Web site at **http://www.latticesemi.com.**

Statements in this news release looking forward in time are made pursuant to the safe harbor provisions of the Private Securities Litigation Reform Act of 1995. Investors are cautioned that forward-looking statements involve risks and uncertainties, including technological and product development risks, market acceptance and demand for our new products, our dependencies on silicon wafer suppliers, the impact of competitive products and pricing, and other risk factors detailed in the Company's Securities and Exchange Commission filings. Actual results may differ materially from forward-looking statements.

**# # #**



For more information contact:

Andy Robin, VP, New Venture Business
Lattice Semiconductor Corporation
**andy.robin@latticesemi.com**
(408)826-6222